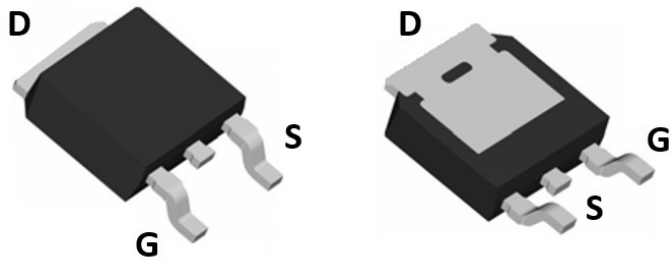
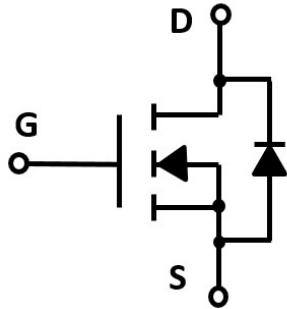


N-Channel Enhancement Mode Field Effect Transistor



TO-252



Product Summary

- V_{DS} 100V
- I_D 15A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) < 115mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) < 130mohm
- 100% UIS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- DC-DC Converters
- Power management functions

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	100	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current	I_D	$T_C=25^\circ\text{C}$	15
		$T_C=100^\circ\text{C}$	10.5
Pulsed Drain Current ^A	I_{DM}	60	A
Single Pulse Avalanche Energy ^B	E_{AS}	9	mJ
Total Power Dissipation	P_D	$T_C=25^\circ\text{C}$	34
		$T_C=100^\circ\text{C}$	17
Thermal Resistance Junction-to-Case ^C	$R_{\theta JC}$	4.4	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+175	$^\circ\text{C}$

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.1	1.8	3.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=8A$		68	115	m Ω
		$V_{GS}=4.5V, I_D=8A$		75	130	
Diode Forward Voltage	V_{SD}	$I_S=15A, V_{GS}=0V$		0.8	1.2	V
Maximum Body-Diode Continuous Current	I_S				15	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V, f=1\text{MHz}$		1070		pF
Output Capacitance	C_{oss}			33		
Reverse Transfer Capacitance	C_{rss}			30		
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=50V, I_D=10A$		26		nC
Gate-Source Charge	Q_{gs}			5.4		
Gate-Drain Charge	Q_{gd}			5.8		
Reverse Recovery Charge	Q_{rr}	$I_F=10A, di/dt=100A/\mu s$		30.1		ns
Reverse Recovery Time	t_{rr}			40		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=50V, R_L=6.4\Omega$ $R_{GEN}=3\Omega$		7		ns
Turn-on Rise Time	t_r			24		
Turn-off Delay Time	$t_{D(off)}$			24		
Turn-off fall Time	t_f			31		

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper

■ Typical Performance Characteristics

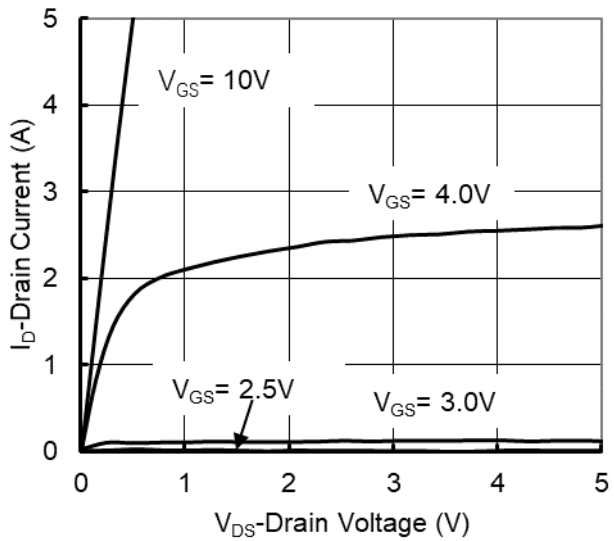


Figure 1. Output Characteristics

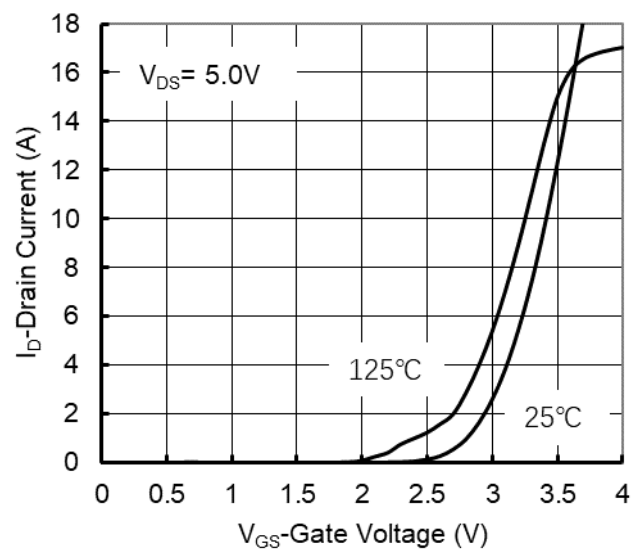


Figure 2. Transfer Characteristics

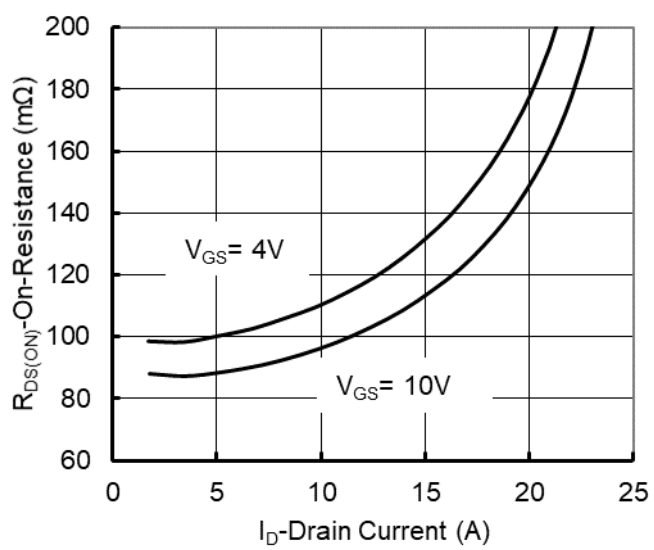


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

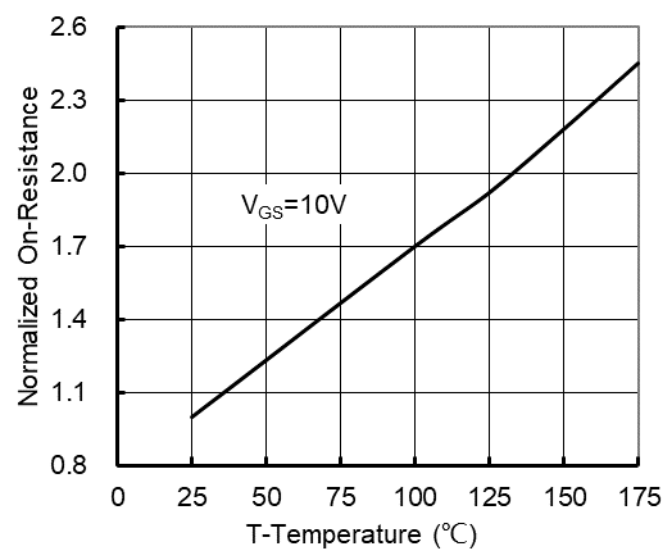


Figure 4. On-Resistance vs. Junction Temperature

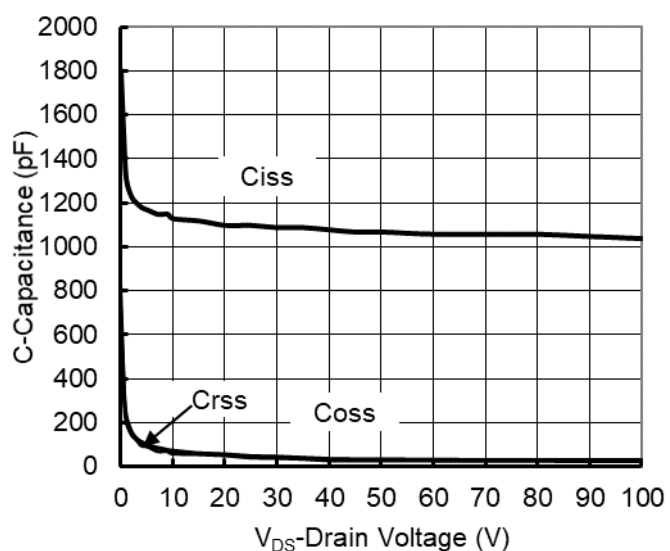


Figure 5. Capacitance Characteristics

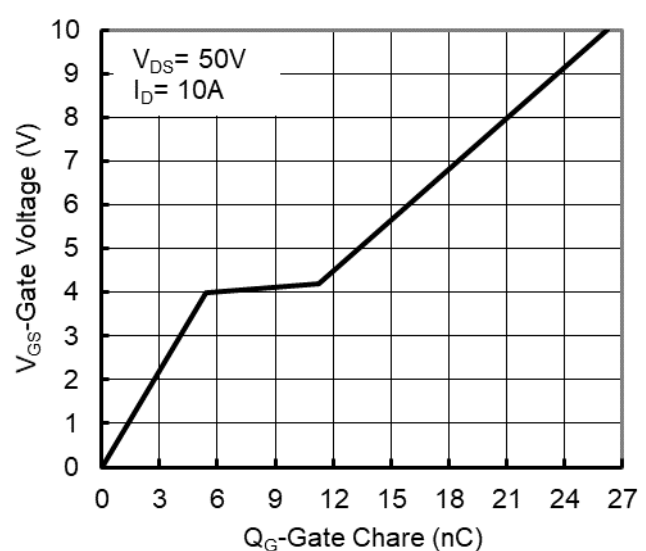


Figure 6. Gate Charge

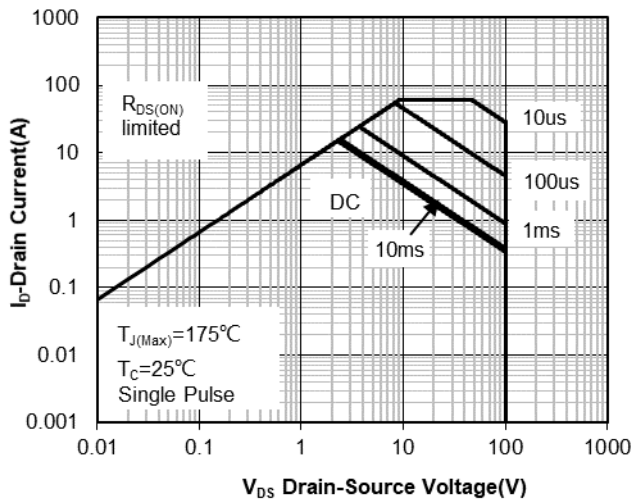


Figure 7. Safe Operation Area

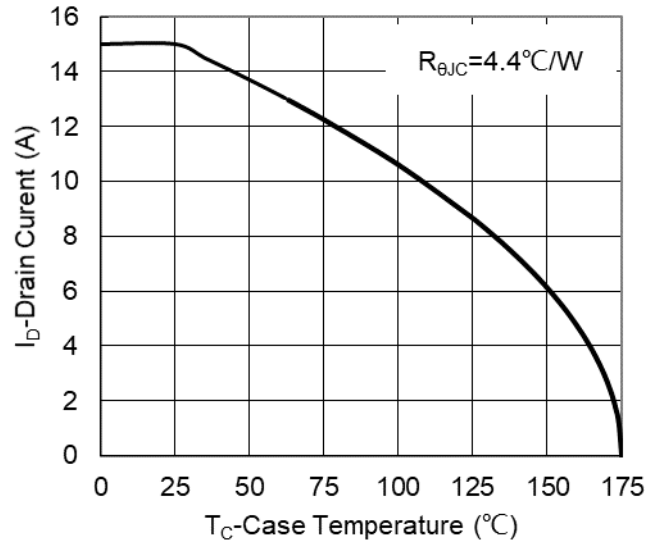


Figure 8. Maximum Continuous Drain Current vs Case Temperature

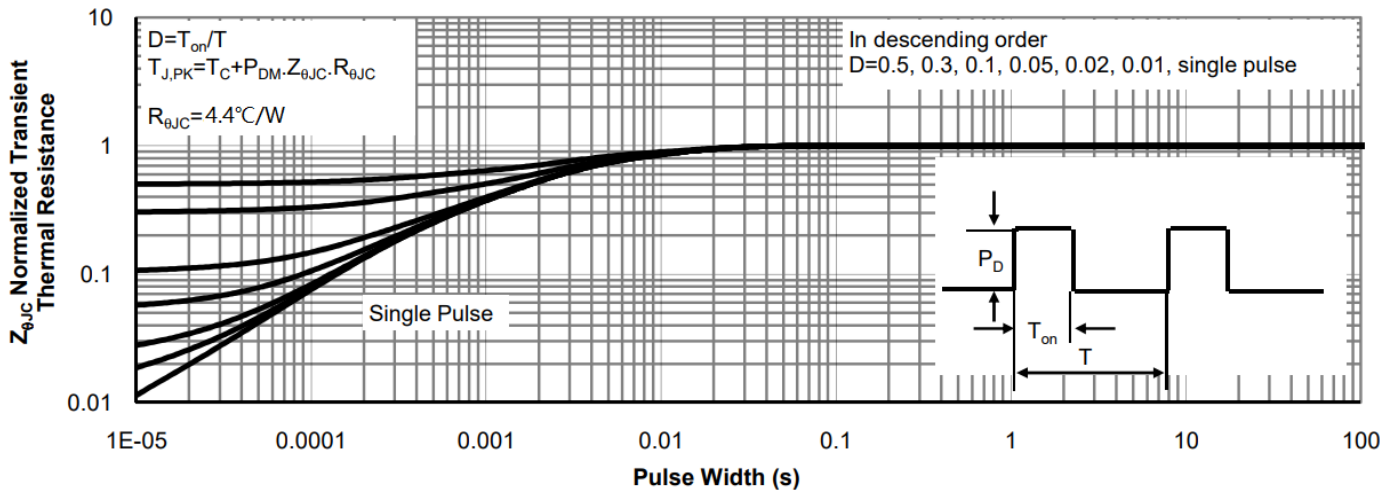
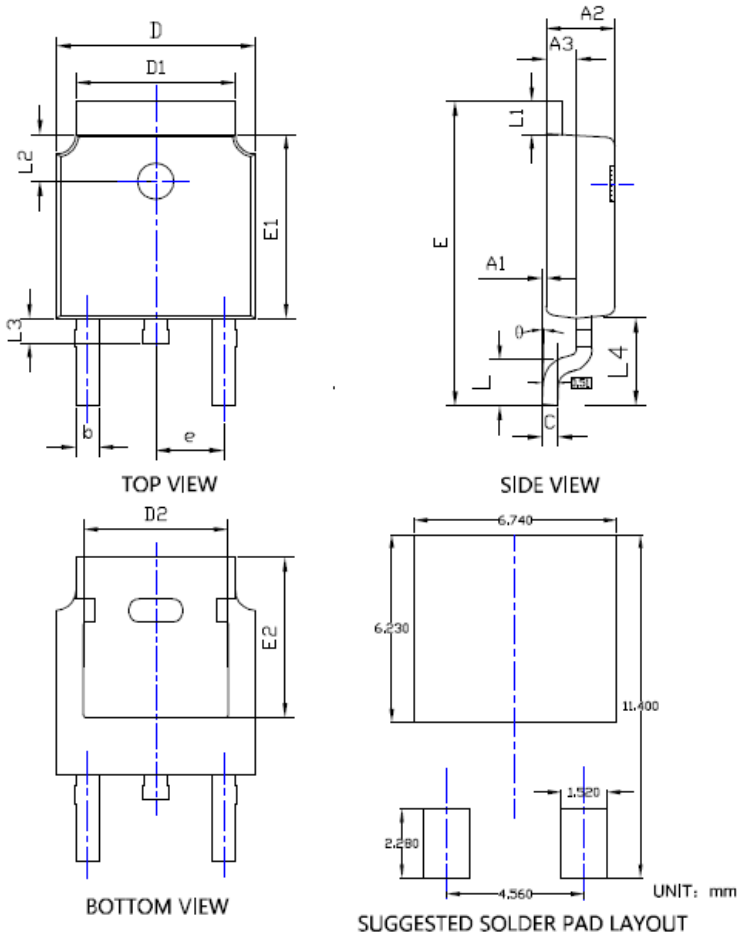


Figure 9. Normalized Maximum Transient Thermal Impedance

■ TO 252 Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
φ	0*	---	10*	0*	---	10*

NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.